REMARKS/ARGUMENTS

Applicants thank the Examiner for the thorough consideration given the present application. Claims 1-15 are pending in the present application. Claims 1, 7, 9, and 11 have been amended. Claims 1 and 11 are independent claims. The Examiner is respectfully requested to reconsider his rejections in view of the Amendments and the following Remarks.

Acknowledgment of Information Disclosure Statement

The Examiner has acknowledged the Information Disclosure Statement filed on December 23, 2003. An initialed copy of the PTO-1449 has been received from the Examiner. No further action is necessary at this time.

Claims 7 and 9 have been amended to correct typographical errors.

Art Rejections Under 35 U.S.C. §§ 102 and 103

In the Office Action, the Examiner rejected claims 11, 12, and 14 under 35 U.S.C. § 102(e) or (a) as being anticipated by U.S. Patent Publication No. 2002/0131442 or European Patent Publication No. 1001648 (collectively "Garg"). The Examiner further rejected claims 1-7, 10, 13, and 15 under 35 U.S.C. § 103(a) as being unpatentable over Garg; and rejected claims 8

and 9 under 35 U.S.C. § 103(a) as being unpatentable over Garg in view of U.S. Patent No. 5,841,771 to Irwin (hereinafter Irwin).

At the outset, Applicants direct the Examiner's attention to claim 1, as amended, which recites a multiplexer receiving a plurality of first bit streams. One of the first bit streams conforms to a first format. Amended claim 1 further recites that the latch is controlled to thereby generate a second bit stream conforming to a second format.

Support for the changes to claim 1 can be found, for example, in the specification at page 30, lines 10-11, which describes cascaded cells including a multiplexer control circuit and latch (Fig. 10) that "*reformat* the input data and latch the input data via latch 1090 prior to passing the input data to the subsequent cell" (emphasis added). A time and space switching ASIC (TISSA) including such cells can be used to "switch data formats between the input and output ports" (page 23, lines 7-8). Thus, in this exemplary embodiment, switching formats between inputs and outputs includes a first input bit stream conforming to a first format and a second output bit stream conforming to a second format. Claim 1, as amended, reflects the subject matter of this exemplary embodiment in the specification.

Claim 11 similarly recites first and second bit streams having first and second formats, and is therefore supported by the specification for the same reasons discussed above in regard to claim 1.

Applicants respectfully traverse the Examiner's rejection of claims 11, 12, and 14 as being anticipated by Garg. Claim 11, as amended, is not anticipated by Garg because the applied references fail to teach each and every element of the claim. In particular, Garg at least fails to teach the claimed method including the steps of receiving a first bit stream conforming to a first format and outputting a second bit stream conforming to a second format, as recited in the amended claim 11.

Garg (2002/0131442) discloses a module receiving eight STS-12 inputs and supplying eight STS-12 outputs (page 5, paragraph 48). As generally understood, "STS-12" designates a particular Synchronous Optical Network ("SONET") format. Accordingly, Garg discloses receiving and outputting bit streams conforming to the same format. Garg fails to teach receipt and output of bit streams with different formats and, thus, necessarily fails to teach the claimed steps of receiving a first bit stream having a first format and outputting a second bit stream having a second format, as recited in claim 11.

In light of the above-described deficiencies of Garg, Applicants submit that claim 11 is allowable over the applied reference and claims 12 and 14 are allowable at least due to their dependency on claim 11.

Applicants respectfully traverse the Examiner's rejection of claims 1-7, 10, 13, and 15 as being unpatentable over Garg. As noted above, amended claim 1 recites the claimed combination of including a multiplexer receiving a first bit stream conforming to a *first format*, and a control circuit controlling a latch to thereby generate a second bit stream conforming to a *second format*. Since Garg is limited to switches that input and output data conforming to the same format, Applicants submit that amended claim 1 is allowable at least for reasons discussed above in regard to claim 11, and claims 2-7 and 10 are allowable at least due to their dependency on claim 1.

With respect to claims 13 and 15, the Examiner acknowledges that Garg fails to teach a programmable space control register, but asserts that this feature would nevertheless be obvious (Office Action at page 4). Applicants respectfully submit, however, that even if such teachings would have been obvious, Garg would still fail to render claims 13 and 15 unpatentable because of the shortcomings discussed above. Claims 13 and 15

are therefore allowable at least due to their dependency on claim 11.

Applicants respectively traverse the Examiner's rejection of claims 8 and 9 under 35 U.S.C. § 103(a) as being unpatentable over Garg in view of Irwin. The Examiner relies on Irwin to allegedly teach a second multiplexer coupled to receive an output signal by another circuit. Such teachings, even if present in Irwin, would nevertheless fail to overcome the above described deficiencies of Garg. Claims 8 and 9, therefore are allowable at least due to their dependency on claim 1.

Conclusion

In light of the foregoing, Applicants respectfully request reconsideration of the present application and a timely allowance of the pending claims.

Should the Examiner believe that any outstanding matters remain in the present application, the Examiner is respectfully requested to contact Jason W. Rhodes (Reg. No. 47,305) at the telephone number of the undersigned to discuss the present application in an effort to expedite prosecution.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,

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